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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,276	02/20/2004	Po-Wei Liu	REAP0050USA	2275

27765 7590 07/12/2006

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EXAMINER
ABRAHAM, ESAW T

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 07/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/708,276	LIU ET AL.	
	Examiner	Art Unit	
	Esaw T. Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/25/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims **1-15** are presented for examination.

Information Disclosure Statement

2. The references listed in the information disclosure statement submitted on 02/25/04 have been considered by the examiner (see attached PTO-1449).

Specification

3. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S. C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims **1-15** are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Brauch et al. (U.S. PN: 6,550,023).

As per claims 1 and 11:

Brauch et al. substantially teach or disclose a semiconductor memory testing, and more particularly to a method and apparatus for testing on-chip RAM and automatically generating a bitmap indicating cell failures (see col. 1, lines 6-9). Brauch et al. teach a method and apparatus that makes it possible to detect and locate failing cells in an integrated circuit memory and further data coming out of the on-chip memory is compared to its expected value while it is still on-chip and in the event of a comparison mismatch (or failure), the results of the comparison and its corresponding address in memory area stored in registers that may be scanned by external hardware and recorded in a bitmap or stored in another on-chip location for later retrieval. Furthermore, Brauch et al. teach that data coming out of on-chip memory is compared to one of two programmable values stored respectively in a pair of respective expected data registers. The result of the compare is placed in a compare results register. Each comparator outputs a 0 if its inputs are the same and a 1 if its inputs are different. If all of the bits in the compare results register are 0, then the data read from memory is the same as the data in the selected expected data register. Conversely, a 1 in the compare results register indicates that memory data does not agree with the selected expected data register. The location of the 1 in the compare results register corresponds to the location of the incorrect memory bit. The outputs of each of the comparators are logically OR'ed together to generate a fault indicator that indicates whether a mismatch occurred in the currently output addressed word in memory. The fault indicator may be used to halt the memory test long enough to scan the contents of the compare results

register and obtain the address in memory that resulted in the fault indication (see col. 2, lines 26-64).

As per claims 2 and 3:

Brauch et al. teach all the subject matter claimed in claim 1 including in a block of an integrated circuit (IC) 2 that contains that includes a memory (4), built-in self-test (BIST) (6) and communication port (8). Further, the BIST functional block (6) is hardware, firmware, or a combination of both, that controls the execution of on-chip memory tests that are designed to detect and locate defects in memory (4) (see col. 3, lines 12-48).

As per claims 4 and 5:

Brauch et al. teach all the subject matter claimed in claim 1 except testing the variance or difference in voltage and temperature. However, the method is inherent to the system of Bauch et al. because, when performing any testing memory devices, the voltage supply and temperature of the system must be put into consideration in order to accurately analyzes test data and stabilizes the production lines.

As per claims 6-10:

Brauch et al. teach all the subject matter claimed in claim 1 including BIST functional block (6) is hardware, firmware, or a combination of both, that controls the execution of on-chip memory tests that are designed to detect and locate defects in memory (4). A fault locator (20) residing within IC 2 performs the comparison between the contents that are read (via data output lines DATA_OUT) and the corresponding expected value. A mismatch between the contents of the addressed location and the

expected value indicates a memory defect that corrupts the cell(s) that map to the mismatching bit(s) of the addressed word. Communication port (8)is used to send mismatch address and comparison result pairs off-chip for storage as comparison mismatches are detected. Alternatively, the comparison mismatch information is stored in a bitmap storage (18) located on-chip for later retrieval by external hardware. The accumulated mismatch pairs at the end of the test comprise a complete bitmap of the precise location of failed cells in memory (4) that were detected by the particular memory test executed by BIST functional block (6) (see col. 3, lines 23-46).

As per claims 12 and 13:

Brauch et al. teach all the subject matter claimed in claim 11 including in a block of an integrated circuit (IC) 2 that contains that includes a memory (4), built-in self-test (BIST) (6) and communication port (8). Further, the BIST functional block (6) is hardware, firmware, or a combination of both, that controls the execution of on-chip memory tests that are designed to detect and locate defects in memory (4) (see col. 3, lines 12-48).

As per claims 14 and 15:

Brauch et al. teach all the subject matter claimed in claim 1 except testing the variance or difference in voltage and temperature. However, the method is inherent to the system of Bauch et al. because, when performing any testing memory devices, the voltage supply and temperature of the system must be put into consideration in order to accurately analyzes test data and stabilizes the production lines.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US PN: 6,857,092 Fox

US PN: 5,051,997 Sakashita et al.

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (571) 272-3812. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for after final communications.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Esaw Abraham

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Art unit: 2133

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